IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(ULL)	
Application Serial No	09/234,233
Filing Date	
nventor	
Assignee Micron T	
Group Art Unit	
Examiner	
Attorney's Docket No	
Title: Semiconductor Processing Methods	

INFORMATION DISCLOSURE STATEMENT

References – See Attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed together with the filing of the Request for Continued Examination (RCE) Application and prior to the receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 11 May 2004

James F. Lake

Reg. No. 44,854

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)

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FILING DATE January 20, 1999 U.S. PATENT DOCUMENTS GROUP 2818												
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	AP		Wolf, S., Silicon Proc	ess., Vol. 2 48-49	and 435							
	AQ											
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EXAMINER DATE CONSIDERED												

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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